27th Reconfigurable Architectures Workshop
May 18–19, 2020 — New Orleans, Louisiana, USA

The 27th Reconfigurable Architectures Workshop (RAW 2020) will be held in New Orleans in May 2020. RAW 2020 is associated with the 34th Annual IEEE International Parallel & Distributed Processing Symposium (IEEE IPDPS 2020) and is sponsored by the IEEE Computer Society and the Technical Committee on Parallel Processing. The workshop is a vibrant forum for researchers to present new ideas, fresh results, and on-going research into both theoretical and practical advances of Reconfigurable Computing.

A reconfigurable computing environment is characterized by the ability of underlying hardware architectures or devices to rapidly alter (often on the fly) the functionalities of their components and the interconnection between them to suit the problem at hand. The area has a rich theoretical tradition and wide practical applicability. There are several commercially available reconfigurable platforms (FPGAs and coarse-grained devices) and many modern applications (including embedded systems and HPC) use reconfigurable subsystems. An appropriate mix of theoretical foundations and practical considerations, including algorithms architectures, applications, technologies and tools, is essential to fully exploit the possibilities offered by reconfigurable computing. The Reconfigurable Architectures Workshop aims to provide a forum for creative and productive interaction for researchers and practitioners in the area. This year the workshop will also provide a platform for work in progress.

Topics of interest

Hot Topics

- Configurable Cloud
- Heterogeneous Computing in Data Centers
- Accelerating Data Center Workloads
- FPGA-based Deep Learning
- Accelerating Genomic Computations
- Accelerating Data Analytics
- Reconfigurable Computing in the IoT era
- Organic Computing, Biologically-Inspired Solutions
- Applications in Finance

Architecture & CAD

- Algorithmic Techniques and Mapping
- Emerging Technologies (optical models, 3D Interconnects, devices)
- Reconfigurable Accelerators
- Embedded Systems and Domain-Specific solutions (Digital Media, Gaming, Automotive applications)
- FPGA-based MPSoC and Multicore
- Distributed Systems & Networks
- Wireless and Mobile Systems
- Critical issues (Security, Energy efficiency, Fault-Tolerance)

Runtime/System Management

- Runtime Reconfiguration Models
- Autonomic computing systems
- Operating Systems and High-Level Synthesis
- High-Level Design Methods (HW/SW co-design, Compilers)
- System Support (Soft processor programming)
- Runtime Support
- Reconfiguration Techniques (reusable artifacts)
- Simulation and Prototyping (performance analysis, verification tools)

Paper Submission

Submissions reporting your latest results, exciting developments and, in special cases, summaries of relevant work are sought. Manuscripts for full papers should not exceed 8 single-spaced, double-column pages using 10-point font on 8.5 x 11 inch pages (IEEE conference style) including references, figures and tables. Manuscripts for short papers should not exceed 4 single-space, double-column pages. Papers are to be submitted through EasyChair. Submitted papers should not have appeared in or be under consideration for another workshop, conference or journal.

Submission deadline	**January 25, 2020**
Decision notification	**February 15, 2020**
Camera-ready papers due	**March 2, 2020**

Organization

Workshop Co-Chairs

Marco D. Santambrogio, Politecnico di Milano
Yu Wang, Tsinghua University

Program Co-Chairs

Oliver Diessel, UNSW Sydney
Christophe Bobda, University of Florida

For current and further information, refer to the RAW'20 website: http://raw.necst.it