.:: May 29, 2017 ::.
08.00 - 08.15: Registration
08.15 - 08.30: Opening
08.30 - 09.30: Keynote 1: **Heterogeneous Technology Configurable Fabrics: Leveraging Reconfiguration as a Pathway Towards Emerging Devices**, Ronald F. DeMara (University of Central Florida, Orlando, FL, USA)
09.30 - 10.00: Short Paper Introduction Session Day 1

14	Godwin Enemali, Adewale Adetomi and Tughrul Arslan. FAReP: Fragmentation-Aware Replacement Policy for Task Reuse on Reconfigurable FPGAs
11	Sonia Alarcon, Marcin Lukowiak and Tejaswini Ananthanarajana. Power Analysis of HLS-Designed Customized Instruction Set Architectures
25	Tajas Ruschke, Lukas Johannes Jung and Christian Hochberger. A Near Optimal Integrated Solution for Resource Constrained Scheduling, Binding and Routing on CGRAs
13	Adewale Adetomi, Godwin Enemali and Tughrul Arslan. Clock Buffers, Nets, and Trees for On-chip Communication: A Novel Network Access Technique in FPGAs

10.00 - 10.30: Coffee Break and Interactive Session Short Papers Day 1

10.30 - 11.45: Session 1: Architectures for Convolutional Neural Networks and Sliding Window

9	Marco Bacis, Giuseppe Natale, Emanuele Del Sozzo and Marco Domenico Santambrogio. A Pipelined and Scalable Dataflow Implementation of Convolutional Neural Networks on FPGA
27	Haruyoshi Yonekawa and Hiroki Nakahara. An On-chip Memory Batch Normalization Free Binarized Convolutional Deep Neural Network on an FPGA
19	Murad Qasaimeh, Phillip Jones and Joseph Zambreno. A Modified Sliding Window Architecture for Efficient BRAM Resource Utilization

11.45 - 12.15: Interactive Session 1

12.15 - 01.15: Lunch

01.15 - 02.55: Session 2: Design and Programming Methods

8	Gary Grewal, Shawki Areibi, Ziad Abouwaimer, Matthew Westrik and Betty Zhao. Automatic Flow Selection and Quality-of-Result Estimation for FPGA Placement
3	Javier Alejandro Varela, Norbert Wehn, Qian Liang and Songyin Tang. Exploiting Decoupled OpenCL Work-Items with Data Dependencies on FPGAs: A Case Study
10	Luca Stornaiuolo, Alberto Parravicini, Gianluca Durelli and Marco Domenico Santambrogio. Exploiting FPGAs from Higher Level Languages A signal analysis case study
26	Philip Gottschling and Christian Hochberger. ReEP: A Toolset for Generation and Programming of Reconfigurable Datapaths for Event Processing

02.55 - 03.25: Interactive Session 2 and Coffee Break

03.25 - 04.15: Session 3: Acceleration of Curran's Approximation and Elliptic Curve Crypto

32	Anna Maria Nestorov, Enrico Reggiani, Marco Domenico Santambrogio, Pavel Burovskiy, Hristina Palikareva and Tobias Becker. A Scalable Dataflow Implementation of Curran's Approximation Algorithm
28	Rabia Shahid, Ted Winograd and Kris Gaj. A Generic Approach to the Development of Coprocessors for Elliptic Curve Cryptosystems

04.15 – 04.35: Interactive Session 3
04.35 - 05.35: Panel: The Role of Reconfigurable Computing Architectures in the era of Cloud Computing and Data Analytics
20.00 – 23.00 Social event at Kone Ichiban Japanese Steakhouse, 8460 Palm Parkway Orlando, FL 32836

.:: May 30, 2017 ::.
08.30 - 09.30: IPDPS Keynote
09.30 - 10.00: Coffee Break
10.00 - 11.00: Keynote 2: **Elastic Dataflow Engines for the Masses**, Georgi Gaydadjiev (VP of Dataflow Software Engineering of Maxeler Technologies)
11.00 - 11:25: Short Paper Introduction Session Day 2

24	Enrico Reggiani, Eleonora D'Arnese, Andrea Purgato and Marco D. Santambrogio. Brain Network acceleration for modeling and mapping of neural interconnections
4	Tripti Jain, Klaus Schneider and Frederik Walk. Out-of-Order Execution of Buffered Function Units in Exposed Datapath Architectures
33	Andres Jacoby and Daniel Llamocca. Dynamic Dual Fixed-Point CORDIC Implementation
23	Emanuele Del Sozzo, Lorenzo Di Tucci and Marco Domenico Santambrogio. A Highly Scalable and Efficient Parallel Design of N-Body Simulation on FPGA
22	Francesca Palumbo, Carlo Sau, Danilo Pani, Paolo Meloni and Luigi Raffo. Real-time Spiking Neural Networks simulation on Swarm Intelligence based digital architecture

11.25 – 11.55: Interactive Session Short Papers Day 2

11.55 - 12.45: Session 4: Acceleration of Biological Signal Processing

7	Luca Cerina, Pierandrea Cancian, Giuseppe Franco and Marco Domenico Santambrogio. A Hardware Acceleration for Surface EMG Non-Negative Matrix Factorization
30	Giovanni Pietro Seu, Paolo Meloni, Giuseppe Tuveri, Gian Nicola Angotzi, Luigi Raffo, Luca Berdondini and Alessandro Maccione. On-FPGA Real-time processing of biological signals from high-density MEAs: a design space exploration

12:45 - 02.10: Lunch

02.10 - 03.00: Session 5: Design Methods

31	Yosi Ben Asher, Esti Stein and Ramachandran Vaidyanathan. Combining Boolean gates and Branching programs in one model can lead to faster circuits
17	Utsav Agarwal and Ramachandran Vaidyanathan. Efficient Totally-Ordered Subset Generation, with Application in Partial Reconfiguration

03.00 - 03.45: Interactive session 4 + 5 and Coffee Break

03.45 - 04.15: Award Session and Closing Remarks