RAW 2016 Program

May 23, 2016	
08.00 - 08.15	Registration
08.15 - 08.30	Opening
08.30 - 09.30	Keynote 1 (Peter Hofstee - IBM, Austin, TX, USA) Session chair: Marco Domenico Santambrogio, Politecnico di Milano, Italy
09.30 - 10.00	**Short Paper Introduction Session Day 1** Session chair: Marco Domenico Santambrogio, Politecnico di Milano, Italy
13	Benedikt Janßen, Moataz Naserddin and Michael Hübner: *A Hardware/Software Co-Design Approach for Control Applications with Static Real-Time Reallocation*
36	Giulia Guidi, Enrico Reggiani, Lorenzo Di Tucci, Gianluca Durelli, Michaela Blott, Marco D. Santambrogio: *On How to Improve FPGA-Based Systems Design Productivity via SDAccel*
14	Jones Y. Mori, Andre Werner, Florian Fricke and Michael Hübner: *A rapid prototyping method to reduce the design time in commercial high-level synthesis tools*
16	Salma Hesham, Diana Göhringer and Mohamed Abd El Ghany: *ARTNoCs: An Evaluation Framework for Hardware Architectures of Real-Time NoCs*
26	Amit Kulkarni, Elias Vansteenkiste, Dirk Stroobandt, Andreas Brokalakis and Antonios Nikitakis: *A fully parameterized Virtual Coarse Grained Reconfigurable Array for High Performance Computing Applications*
4	Anita Tino and Kaamran Raahemifar: *Assessing Multi-Task Placement Algorithms in RCUs*
10.00 - 10.30	Coffee Break and Interactive Session Short Papers Day 1
10.30 - 11.45	**Session 1: Application Mapping and Design Space Exploration** Session chair: Brian Veale, IBM, USA
15	Lester Kalms and Diana Göhringer: *Clustering and Mapping Algorithm for Application Distribution on a Scalable FPGA Cluster*
42	Syed Waqar Nabi and Wim Vanderbauwhede: *A Fast and Accurate Cost Model for FPGA Design Space Exploration in HPC Applications*
2	Hyunsuk Nam and Roman Lysecky: *Latency, Power, and Security Optimization in Distributed Reconfigurable Embedded Systems*
11.45 - 12.15	Interactive Session 1
12.15 - 13.15	Lunch
13.15 - 14.55	**Session 2: Applications** Session chair: Steve Wilton, University of British Columbia, Canada
45	Daniel Llamocca and Daniel Aloi: *A Reconfigurable Fixed-Point Architecture for Adaptive Beamforming*
37	Aaron Mills, Phillip H. Jones and Joseph Zambreno: *Parameterizable FPGA-based Kalman Filter Coprocessor Using Piecewise Affine Modeling*

47	Chi Zhang, Ren Chen and Viktor Prasanna: *High Throughput Large Scale Sorting on a CPU-FPGA Heterogeneous Platform*
21	Juan Andrés Pérez-Celis, José Martínez-Carranza, Alicia Morales-Reyes, Claudia Feregrino-Uribe and René Cumplido: *An FPGA Architecture to Accelerate the Burrows Wheeler Transform by Using a Linear Sorter*
14.55 - 15.25	Interactive Session 2 and Coffee Break
15.25 - 16.40	**Session 3: Processor Architectures** Session chair: Rene Cumplido, INAOE, Mexiko
24	Mohamed El-Hadedy, Hristina Mihajloska, Danilo Gligoroski, Amit Kulkarni, Dirk Stroobandt and Kevin Skadron: *A 16-bit Reconfigurable Encryption Processor for Pi-Cipher*
35	Stephan Nolting, Guillermo Paya-Vaya, Florian Giesemann, Holger Blume, Sebastian Niemann and Christian Müller-Schloer: *Dynamic Self-Reconfiguration of a MIPS-Based Soft-Processor Architecture*
12	Steffen Vaas, Marc Reichenbach and Dietmar Fey: *An Application-specific Instruction Set Processor for Power Quality Monitoring*
16.40 – 17.00	Interactive Session 3
17.00 - 18.00	**Panel** Session chair: Marco Domenico Santambrogio, Politecnico di Milano, Italy
21.00 – 24.00	RAW 2016 social event at **Kingstone Mines, 2548 North Halsted Street, Chicago, IL 60614**. Sponsored by **TOPIC**.

May 24, 2016	
08.30 - 09.30	IPDPS Keynote
09.30 - 10.00	Coffee Break
10.00 - 11.00	Keynote 2 (Patrick Lysaght - Xilinx, San Jose, CA, USA) Session chair: Juergen Becker, Karlsruhe Institute of Technology, Germany
11.00 - 11:25	**Short Paper Introduction Session Day 2** Session chair: Emanuele Del Sozzo, Politecnico di Milano, Italy
44	Alexandra Kourfali and Dirk Stroobandt: *Efficient Hardware Debugging using Parameterized FPGA Reconfiguration*
10	Fynn Schwiegelshohn, Florian Kästner and Michael Hübner: *Enabling Dynamic Reconfiguration of Numerical Methods for the Robotic Motion Control Task*
28	Martin Letras, Raudel Hernández-León and Rene Cumplido: *Hardware Architectures for Frequent Itemset Mining Based on Equivalence Classes Partitioning*
19	Fabiola Casasopra, Gea Bianchi, Gianluca C. Durelli and Marco D. Santambrogio: *Parallel Protein Identification Using an FPGA-Based Solution*
3	Nikolaos Stekas and Dirk van den Heuvel: *Face recognition using Local Binary Patterns Histograms (LBPH) on an FPGA-based System on Chip (SoC)*

11:25 - 11:55	Interactive Session Short Papers Day 2
11.55 - 13.10	**Session 4: Scheduler and Runtime Systems** Session chair: Claudia Feregrino, INAOE, Mexiko
23	Andrea Purgato, Davide Tantillo, Marco Rabozzi, Donatella Sciuto and Marco D. Santambrogio: *Resource-Efficient Scheduling for Partially-Reconfigurable FPGA-based Systems*
31	Tajas Ruschke, Lukas Johannes Jung, Dennis Wolf and Christian Hochberger: *Scheduler for Inhomogeneous and Irregular CGRAs with Support for Complex Control Flow*
20	Jens Rettkowski, Philipp Wehner, Evgheni Cutiscev and Diana Goehringer: *LinROS: A Linux-based Runtime System for Reconfigurable MPSoCs*
13.10 - 14.15	Lunch
14.15 - 15.15	Keynote 3 (Dirk van den Heuvel - TOPIC Embedded Products, Eindhoven, the Netherlands) Session chair: Ramachandran Vaidyanathan, Louisiana State University, USA
15.15 - 15.45	Interactive session 4 and Coffee Break
15.45 - 17.00	**Session 5: High Level Synthesis and Object-Oriented Programming** Session chair: Diana Goehringer, Ruhr-University Bochum, Germany
17	Emanuele Del Sozzo, Andrea Solazzo, Antonio Miele and Marco D. Santambrogio: *On the Automation of High Level Synthesis of Convolutional Neural Networks*
18	Gianluca C. Durelli, Fabrizio Spada, Christian Pilato and Marco D. Santambrogio: *Scala-based Domain-Specific Language for Creating Accelerator-based SoCs*
22	Hongyuan Ding, Sen Ma, Miaoqing Huang and David Andrews: *OOGen: An Automated Generation Tool for Custom MPSoC Architectures Based on Object-oriented Programming Methods*
17.00 - 17.20	Interactive session 5
17.20 - 17.55	Award Session and Closing Remarks