On How to Improve FPGA-Based Systems Design Productivity via SDAccel

Giulia Guidi, Enrico Reggiani, Lorenzo Di Tucci,
Gianluca Durelli, Michaela Blott, Marco D. Santambrogio
Politecnico di Milano, Dipartimento di Elettronica, Informazione e Bioingegneria, Milano, Italy
Xilinx Research, Dublin, IE

Issue & Idea

Custom **hardware accelerators** are widely used to:

- improve the performance in terms of execution times;
- reduce energy consumption.

Issues…

The hardware design flow is:

- hard;
- time consuming;
- error prone.

…as new opportunities!

The latest toolchain by Xilinx, SDAccel, aims at simplifying the design flow. Our work's **goal** is the validation of SDAccel potentialities from the user's point of view.

Case studies

- ## Protein folding

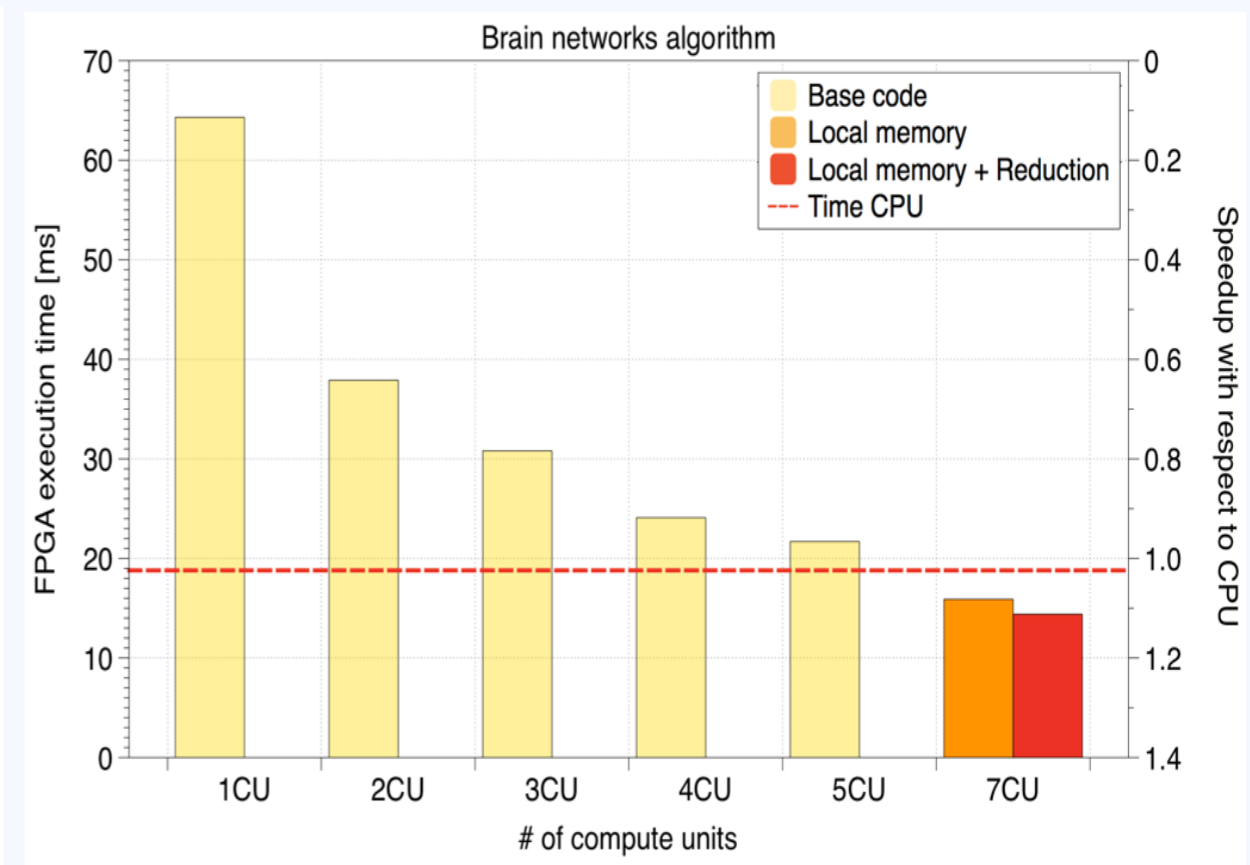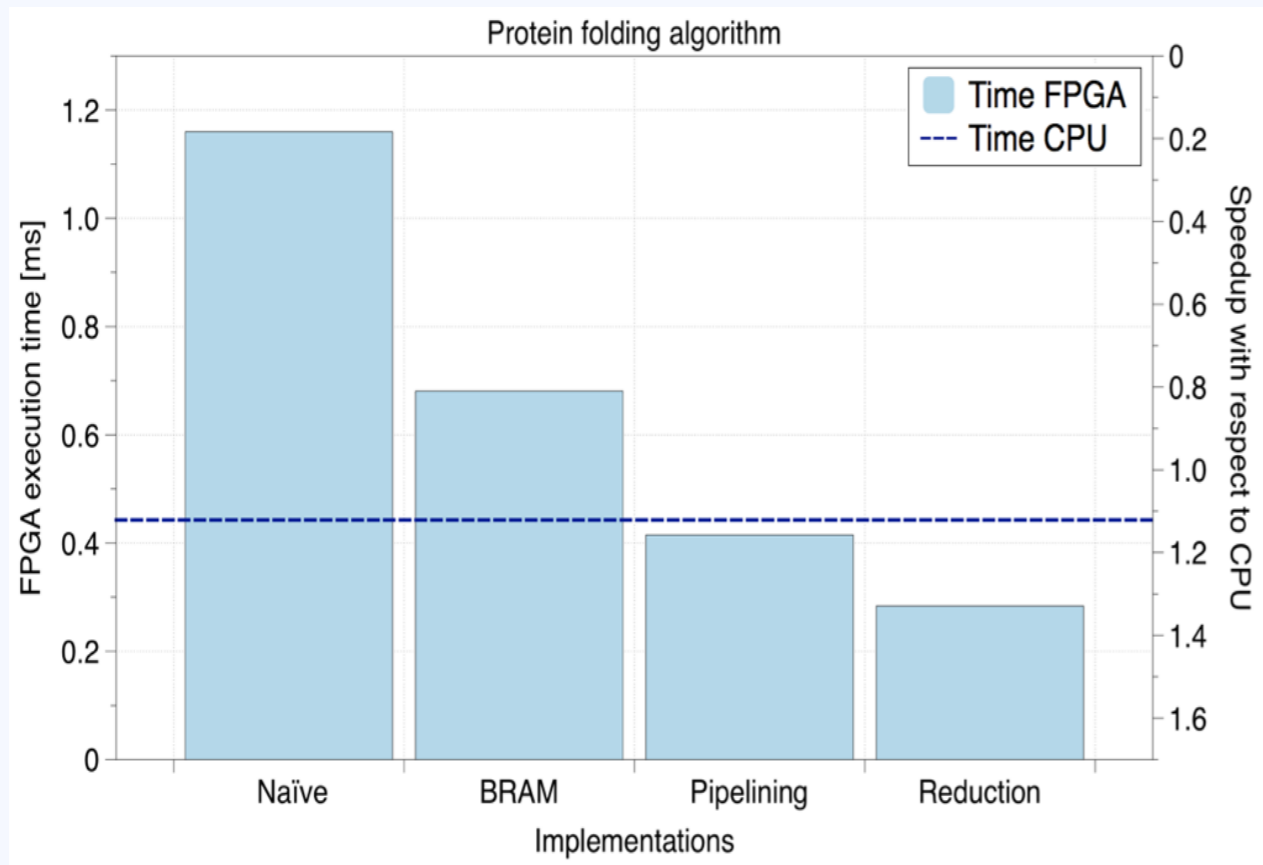 Is the physical process by which a sequence of amino acids in a protein folds into its 3D structure.
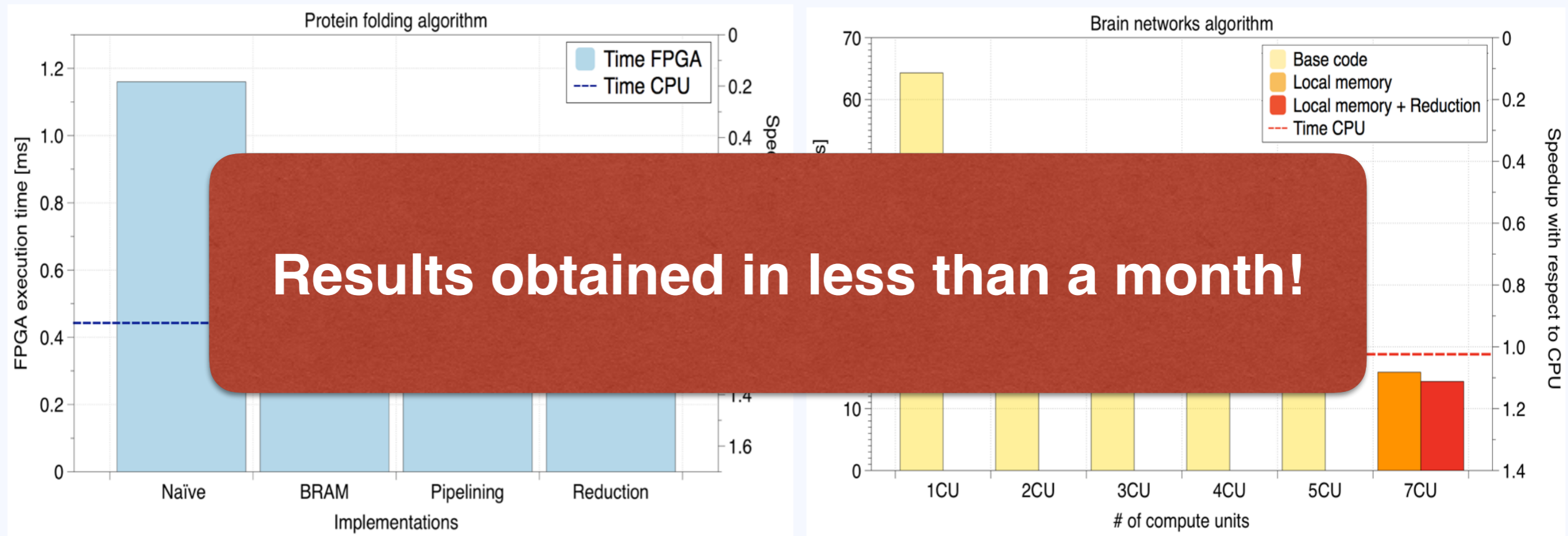
- ## Brain Networks

  Define the correlation between groups of neurons of a brain under stimulation.

Issue: high computational costs of the algorithms

Results
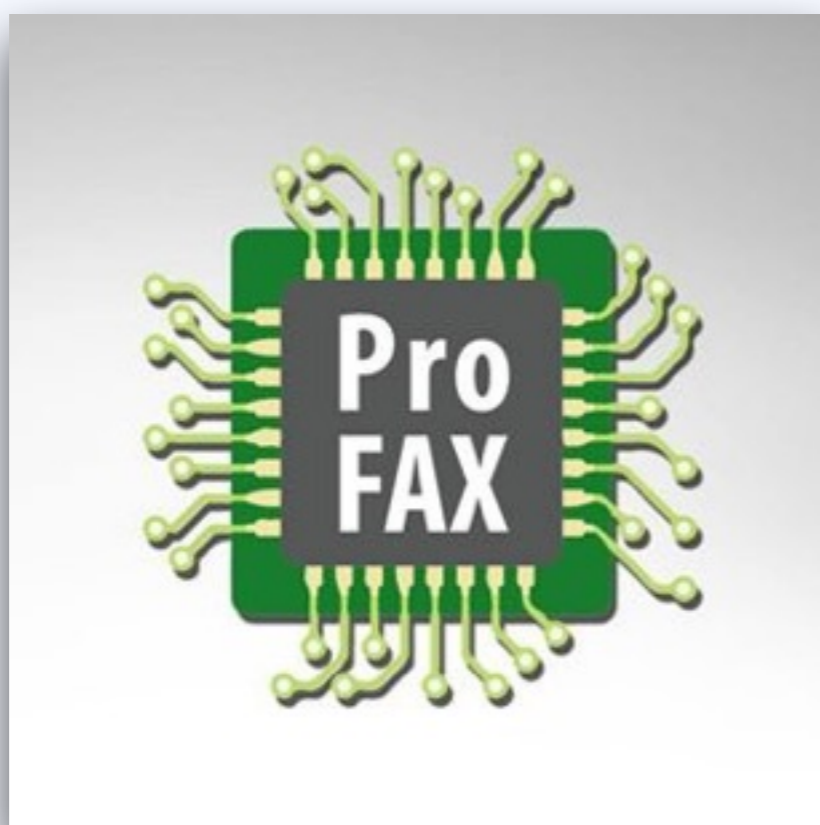
Results

Results obtained in less than a month!

SDAccel seems to be a **promising instrument** for supporting the hardware design flow.

Follow up projects

The two case studies presented here are competing for the
Xilinx Open Hardware 2016

https://www.facebook.com/profaxnecstlab/   https://www.facebook.com/BrainNECSTwork/

https://twitter.com/ProFAX_NECST   https://twitter.com/Brain_NECSTwork

https://www.youtube.com/channel/UCaovqRpUc7D_Uf2WJHL0rvA

Thanks for your attention

Questions?

Giulia Guidi, Enrico Reggiani, Lorenzo Di Tucci,
Gianluca Durelli, Michaela Blott, Marco D. Santambrogio
Politecnico di Milano, Dipartimento di Elettronica, Informazione e Bioingegneria, Milano, Italy,
{*enrico2.reggiani, lorenzo.ditucci, giulia.guidi*}@mail.polimi.it
{*gianlucacarlo.durelli, marco.santambrogio*}@polimi.it
Xilinx Research, Dublin, IE
michaela.blott@xilinx.com