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ARTNoCs: An Evaluation Framework for Hardware Architectures of Real-Time NoCs

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GUC
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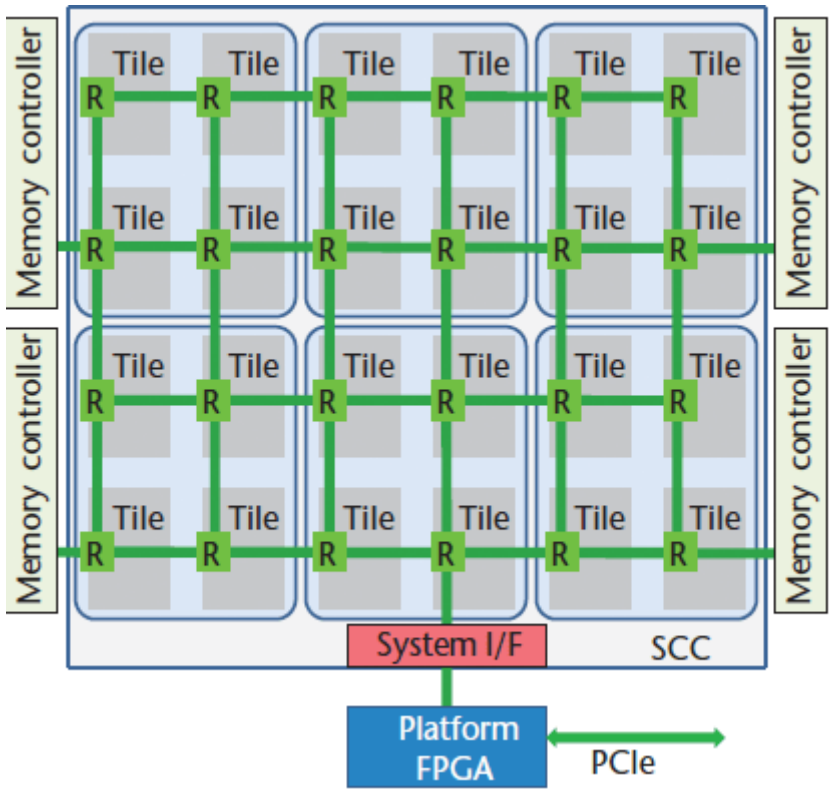
الجامعة الألمانية بالقاهرة

Motivation

- **NoC-based MPSoCs**
  Typical fit for embedded systems

- **Embedded Systems**
  ⇒ **Real-Time Requirements**
  - Time + Correctness
  - Hard RT: e.g. Avionics
  - Soft RT: e.g. Streaming

- **Real-Time NoCs**
  - Predictable Behavior
  - Performance Guarantees
  - Transmission Latency < deadline
  - Quality of Service (QoS) NoCs



Intel 48-Core Single-Chip Cloud Computer in 2D Mesh

T. Mattson et al., "The 48-core SCC Processor: the Programmer's View," in SC10, 2010.

Background

NoC Architectures for Real-Time Guarantees using:

1. Circuit-Switching
2. Packet-Switching
3. Table-Switching
4. Hybrid-Switching

- **Architectural solutions lack common**
  - ⇒ **Evaluation Platform**
  - ⇒ **Performance Criteria**
  - ⇒ **Evaluation Parameters**

- **NoC Comparisons**
  - ⇒ **Vague contreversy ➔ Several simulating environments**

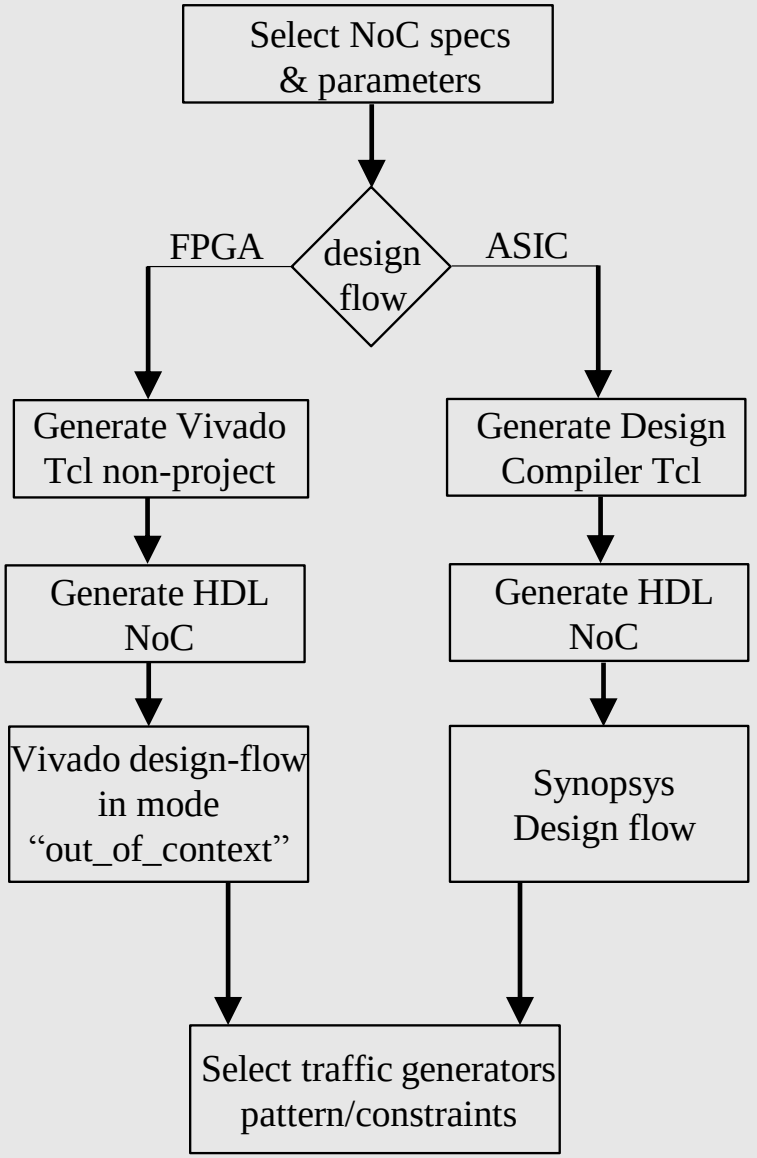
State-of-the-art

Specifications		BookSim [6]	ATLAS [7]	CONNECT [8]	DRNoC [9]	DART [10]	**This work**
Simulator type		Cycle acc.	RTL	RTL	RTL	RTL	RTL
FPGA flow		-	✓	✓	✓	✓	✓
ASIC flow		-	-	-	-	-	✓
Supported architecture	VC-PS-router	✓	✓	✓	✓	✓	✓
	TDM-router	-	-	-	-	-	✓
	CS-router	-	-	-	-	-	✓
Evaluation parameters	Latency	✓	✓	✓	✓	✓	✓
	Power	-	✓	-	-	-	✓
	Area	-	✓	✓	✓	✓	✓
	Speed	-	✓	✓	✓	✓	✓
	QoS level	-	-	-	-	-	✓
	Test Traffic	synthetic	synthetic	synthetic	synthetic	synthetic	synthetic

ARTNoCs Design Flow

ARTNoCs:

- **First hardware evaluation framework for Real-Time NoCs.**
- **Design exploration of QoS router architectures on a reliable evaluation platform.**
- **A modular router architecture for flexible plug-and-play of different router modules**



Evaluation Results

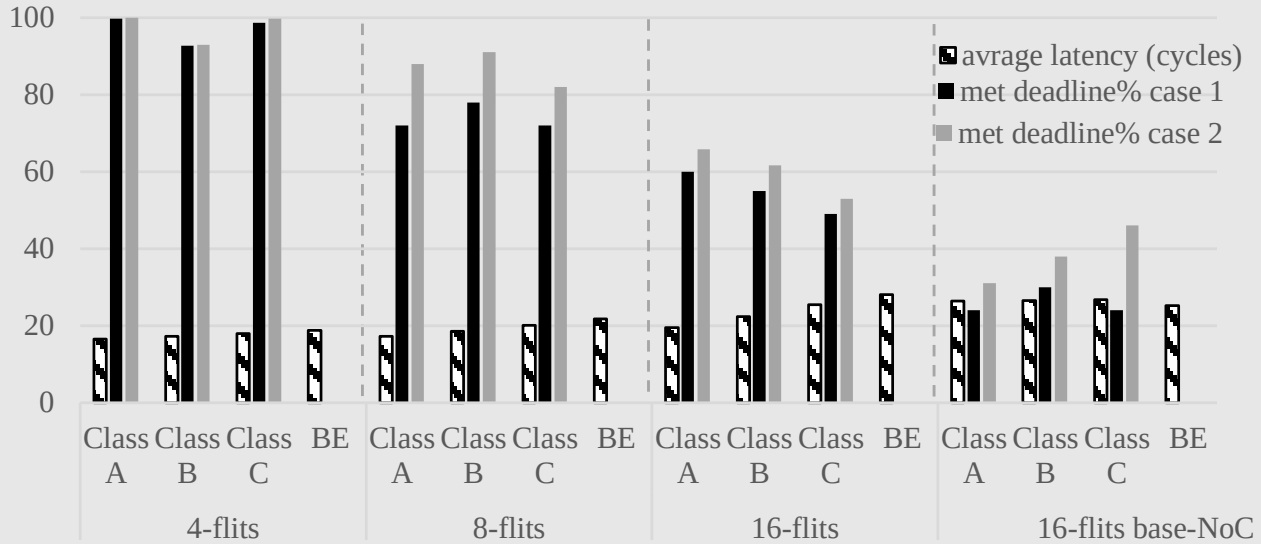
Results for a 32-bit VC-based Packet-Switched NoC with 4 fixed priority levels (QNoC [12]):

Hardware results:

Eval. Param.	4x4 PS-NoC_4	Router
FPGA results		
LUT	62,646	1,925
Slices	22,549	1,221
Freq. (MHz)	125.6	232
Power dyn (W)	0.297	0.075
ASIC results		
Area (mm^2)	9.14	0.32
Freq. (MHz)	74.6	98
Power dyn (mW)	4.62	0.51
Power leak (mW)	33.5	1.2155

Latency & QoS results:

3x3 mesh NoC under Uniform random traffic constrained by 3 hops.



Conclusion

ARTNoCs:

- **The first hardware framework targeting real-time NoCs.**
- **Supports a modular structure for design exploration of QoS-router architectures.**
- **It evaluates for a selected real-time router architecture:**
  - **FPGA hardware performance**
  - **ASIC hardware Performance**
  - **latency performance**
  - **deadline committment for a specified traffic scenario**