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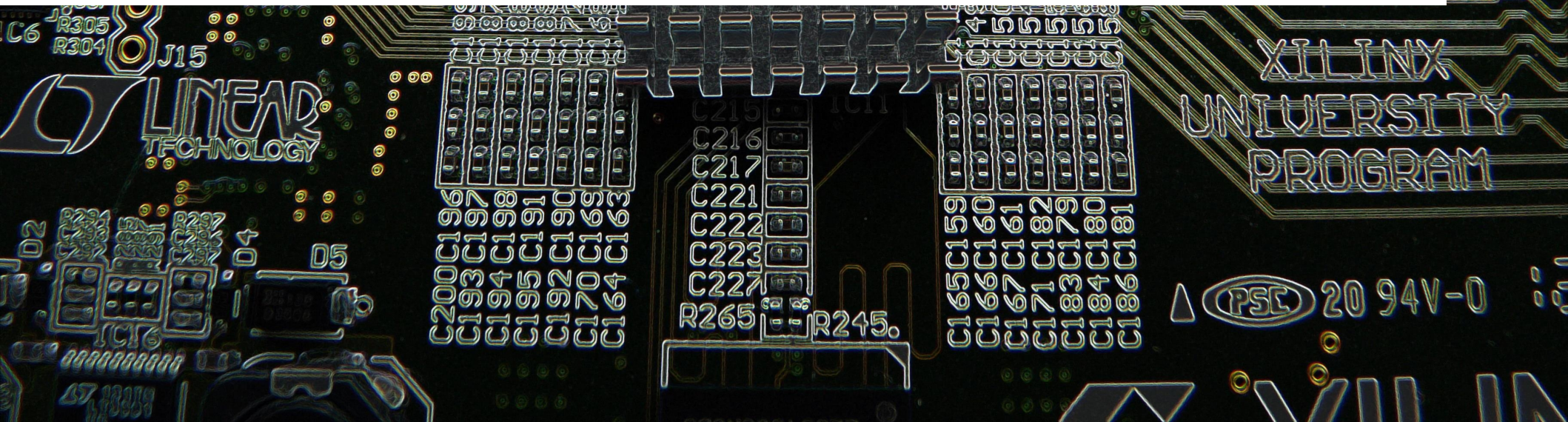
A rapid prototyping method to reduce the design time in commercial high-level synthesis tools

Jones Silva, André Werner, Florian Fricke, Michael Hübner

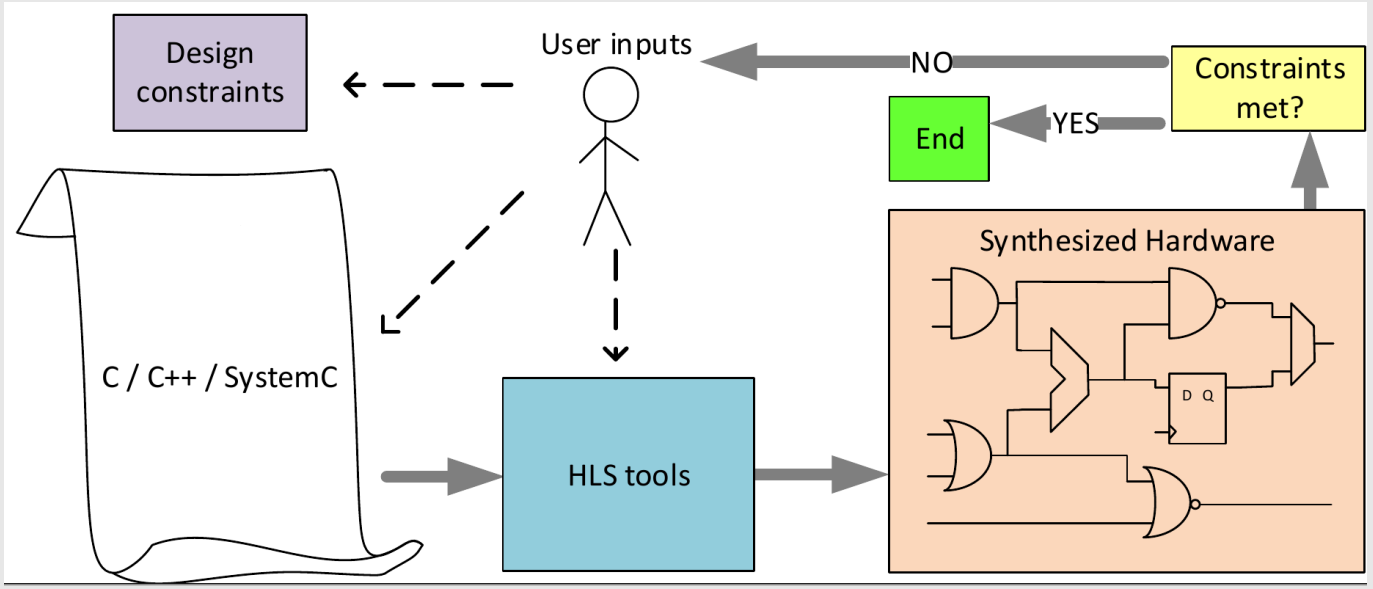
E S I T

Lehrstuhl für Eingebettete Systeme der Informationstechnik (ESIT)
Fakultät für Elektrotechnik und Informationstechnik
Prof. Dr.-Ing. habil. Michael Hübner

www.esit.rub.de

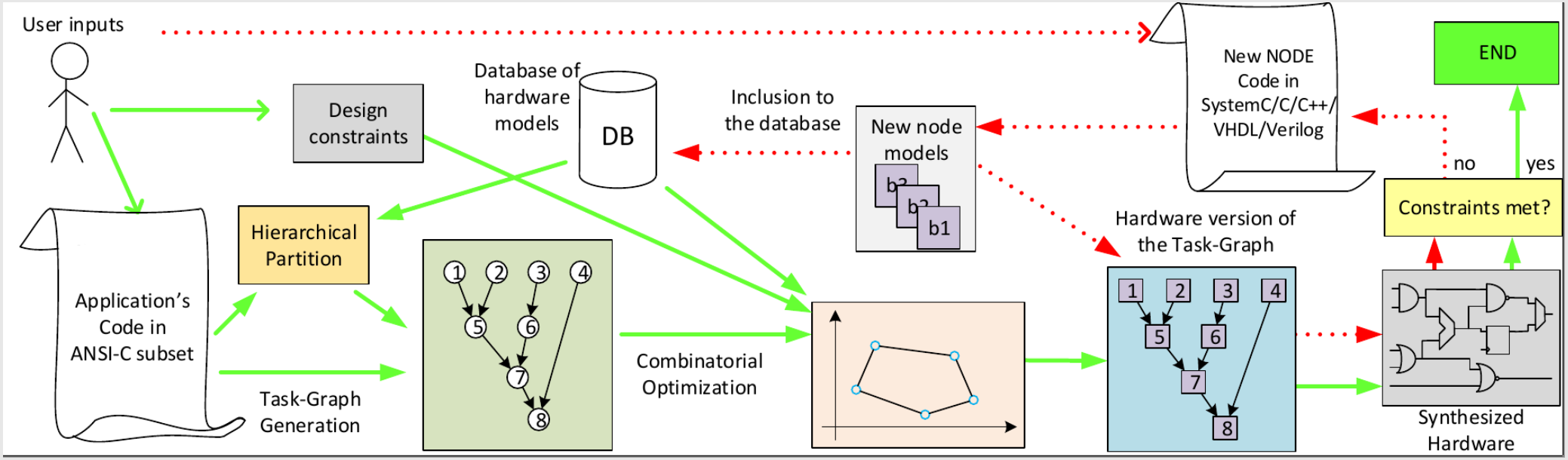


Motivation



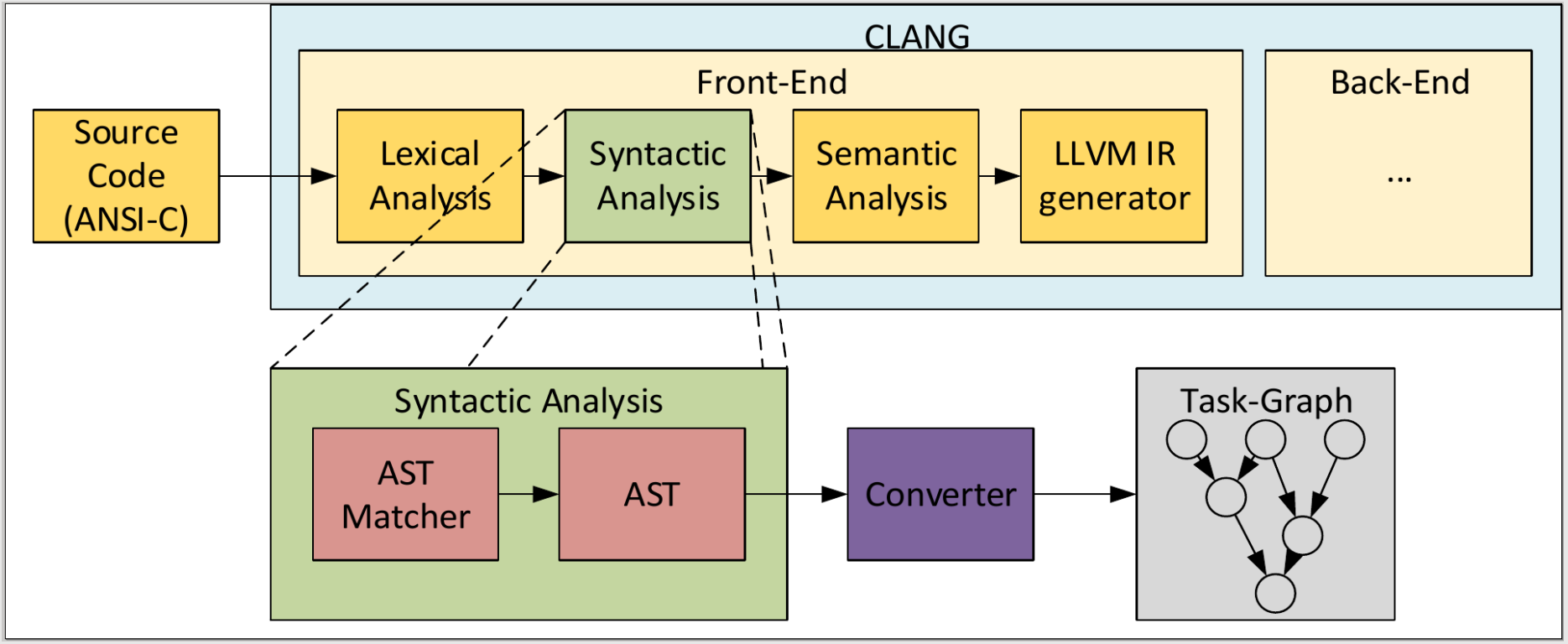
- Standard flow requires too much user interaction.
- Not suitable for non-experienced users.
- How to speed-up the user access to a “good” design?

Proposed solution



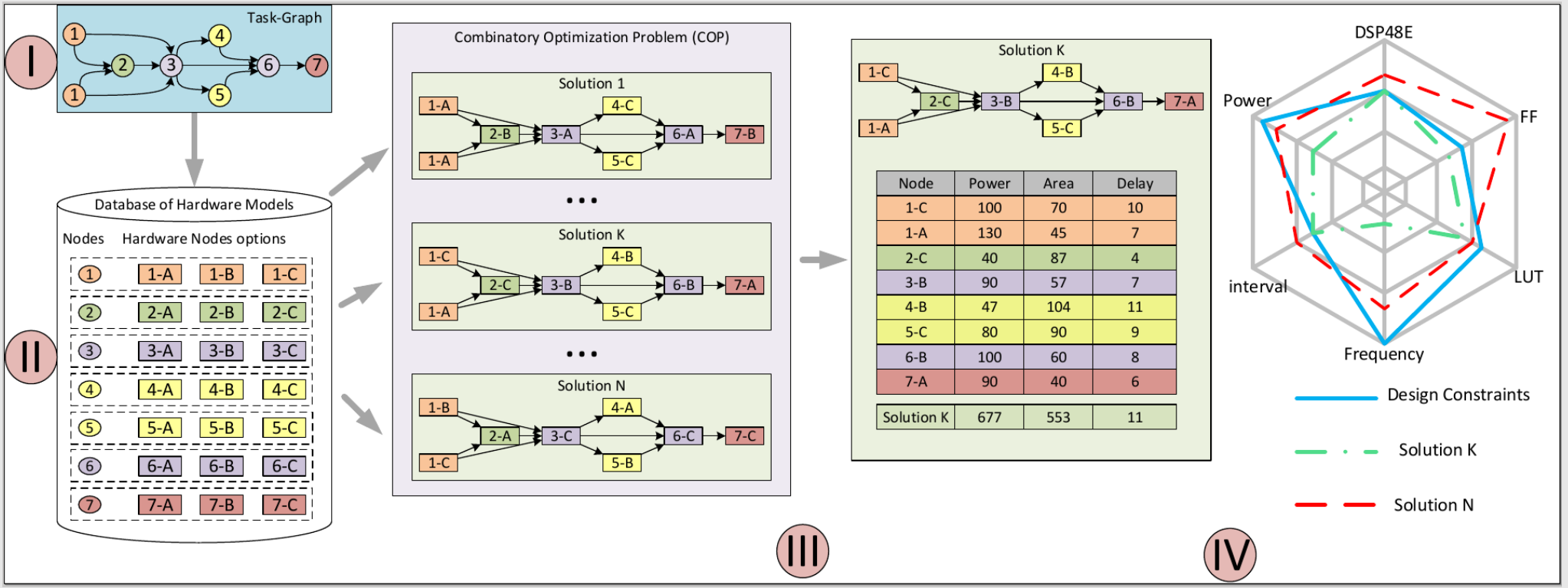
- Minimize non-experienced user's interaction
- Use Pre-Characterized blocks

Task-Graph creation



- LLVM Framework
- Static Analysis
- From AST to Task-Graph

Search problem



- Pre-Characterized node models (Database)
- Combinatorial problem
- Final solution depends on the design constraints

Conclusion

TABLE I. ALTERNATIVE HARDWARE NODES ON THE XILINX XC7VX690TFFG1761-2 FPGA DEVICE

Node name	DSP48E	FF	LUT	Freq. (MHz)	interval (cycles)	Power (mW)
add-v1	0	0	32	537	1	1
add-v2	1	0	0	443	1	1
mult-v1	3	20	18	242	6	5
mult-v2	3	19	17	242	1	6
mac-v1	3	53	49	246	4	5
mac-v2	3	148	49	243	1	7
simpleIF-v1	0	0	32	373	3	1
simpleIF-v2	0	2	16	118	2	1
simpleFOR-v1	0	0	28	332	5	1
simpleFOR-v2	0	8	10	289	2	1

TABLE II. RESULTS OF DIRECT IMPLEMENTATIONS AND OF OUR METHOD ON THE XILINX XC7VX690TFFG1761-2 FPGA DEVICE

	Version	DSP 48E	FF	LUT	Freq. (MHz)	interval (cycles)	Power (mW)
convolution	direct imp.1	30	497	309	215	7	44
	direct imp.2	30	814	306	222	1	57
	conv-add1-mult1	27	180	418	224	7	51
	conv-add1-mult2	27	153	391	183	2	51
	conv-add2-mult1	35	153	135	214	2	54
	conv-add2-mult2	35	168	112	202	2	55
	pred-conv-add2-mult2	35	171	153	242	2	62
	conv-mac1	37	136	450	228	4	32
	conv-mac2	27	477	450	238	1	44
fibo.	direct imp.	0	129	128	156	5	4
	generated	0	152	115	167	9	6

- The results indicate feasibility of the solution for small systems.
- Selected solutions are compatible with HLS results after some user's interaction.
- Scalability must be determined with bigger systems.